Patent claims

1. A semiconductor power switch (1, 20, 30) having:
- a source contact (2),
- a drain contact (3),
- a semiconductor structure which is provided between the source contact (2) and the drain contact (3), and
- a gate (5) which can be used to control a current flow through the semiconductor structure between the source contact (2) and the drain contact (3),

wherein
the semiconductor structure has a plurality of nanowires (4) which are connected in parallel and are arranged in such a manner that each nanowire (4) forms an electrical connection between the source contact (2) and the drain contact (3).

2. The semiconductor power switch (1, 20, 30) as claimed in claim 1,
wherein
the length of the nanowires (4) is ((0.2 m) * (maximum value of the voltage (in V) which is applied to the semiconductor power switch)).

3. The semiconductor power switch (1) as claimed in claim 1 or 2,
wherein
the gate (5) is implemented in the form of a gate layer which is provided between the source contact (2) and the drain contact (3) and is permeated by the nanowires (4), the nanowires (4) being electrically insulated from the gate layer (5).

4. The semiconductor power switch (20, 30) as claimed in either of claims 1 and 2,
wherein

the gate (5) is implemented in the form of a plurality of gate bands (5') whose longitudinal orientation respectively runs essentially perpendicular to the orientation of the nanowires (4) and whose transverse orientation corresponds to the orientation of the nanowires (4), the nanowires being electrically insulated from the gate (5').

5. The semiconductor power switch (1, 20, 30) as claimed in claim 4,
wherein
the nanowires (4) run within trenches (21) which are provided between the gate bands (5').

6. The semiconductor power switch (1, 20, 30) as claimed in claim 4 or 5,
wherein
the gate bands (5') and/or trenches (1) are at an equal distance from one another.

7. The semiconductor power switch (1, 20, 30) as claimed in claim 5 or 6,
wherein
tubes (24) are provided within the trenches (21), at least one nanowire (4) respectively running within said tubes.

8. The semiconductor power switch (1, 20, 30) as claimed in one of claims 5 to 7,
wherein
insulation layers (22) are provided between the trenches (21) and the gate bands (5').

9. The semiconductor power switch (1, 20, 30) as claimed in one of the preceding claims,
wherein
the nanowires (4) are insulated from one another.

10. The semiconductor power switch (1, 20, 30) as claimed in one of the preceding claims,
wherein
the nanowires (4) are at an equal distance from one another.

11. The semiconductor power switch (1, 20, 30) as claimed in one of claims 3 to 10,
wherein
the gate layer/the gate bands (5, 5') has/have a layer thickness/band width which is approximately 1/3 of the distance between the source contact (2) and the drain contact (3).

12. The semiconductor power switch (30) as claimed in one of claims 4 to 10,
wherein
each gate band (5') is split into a plurality of gate subbands (5'') which are insulated from one another, the gate subbands (5'') being arranged above one another and each being designed such that it can be driven individually.

13. The semiconductor power switch (30) as claimed in claim 12,
wherein
the gate subbands (5'') of a gate band (5') are at an equal distance from one another.

14. The semiconductor power switch (30) as claimed in claim 13,
wherein
the vertical positions of the gate subbands (5'') of a gate band (5') are shifted with respect to the vertical positions of the gate subbands (5'') of an adjacent gate band (5').

15. The semiconductor power switch (1, 20, 30) as claimed in one of the preceding claims,
wherein
the nanowires (4) are semiconducting carbon nanotubes.

16. The semiconductor power switch (1, 20, 30) as claimed in one of the preceding claims,
wherein
the nanowires (4) contain

- silicon;
- germanium;
- at least one of the III-V semiconductors BN, BP, BAs, AlN, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InN, InP, InAs, InSb;
- at least one of the II-VI semiconductors ZnO, ZnS, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, HgSe, HgTe, BeS, BeSe, BeTe, MgS, MgSe;
- at least one of the compounds GeS, GeSe, GeTe, SnS, SnSe, SnTe, PbO, PbS, PbSe, PbTe,
- at least one of the compounds CuF, CuCl, CuBr, CuI, AgF, AgCl, AgBr, AgI.

17. The semiconductor power switch (1, 20, 30) as claimed in claim 15 or 16,
wherein
the nanowires (4) are p-doped or n-doped.

18. A method for improving the blocking effect of a semiconductor power switch as claimed in one of claims 12 to 17,
wherein,
in the blocked state, the potentials of the gate subbands (5'') are selected in such a manner that the band gap structures of the nanowires assume an undulating shape.

19. A method for producing a semiconductor power switch, said method having the following steps of:

- forming a layer structure on a drain contact (3), said layer structure having a first insulation layer (7), a gate layer (5) which is arranged above the latter and a second insulation layer (8) which is arranged above the gate layer,
- forming trenches (21) in the layer structure, said trenches reaching as far as the drain contact (3),
- forming nanowires (4) within the trenches (21),
- forming a source contact (2) on the top side of the layer structure.

20. The method for producing a semiconductor power switch as claimed in claim 19,
which comprises
the following steps of:

- forming first trenches (25) in the layer structure,
- filling the first trenches (25) with gate oxide (22),
- forming second trenches (26) in the gate oxide, the second trenches (26) reaching as far as the drain contact (3),
- forming nanowires (4) within the second trenches (26),
- forming a source contact (2) on the top side of the layer structure.

21. The method as claimed in claim 19 or 20,
wherein
the drain contact (3) is composed of molybdenum or tantalum or contains these materials.

22. The method as claimed in claim 21,
wherein
a catalyst is deposited on the molybdenum or tantalum before the layer structure is formed or before the nanowires are formed.